AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning at page 2, line 3, with the following rewritten paragraph:

The problem of substrate noise can be particularly problematic in mixed signal IC designs. In such designs, substrate noise analysis is essential for avoiding any performance degradation or failure due to the noise coupled through the substrate from the noisy ~~nosy~~ digital circuits, i.e, the digital core, to the sensitive analog circuits. It is also important to analyze mixed signal IC designs for substrate noise sensitivity early in the design cycle, so that the design teams have sufficient time to take steps to create effective on-chip electrical isolation strategy without extensive and costly re-design cycles.

Please replace the paragraph beginning at page 7, line 21, with the following rewritten paragraph:

In the preferred embodiment, the steps taken to estimate the noise generated by the core circuits are as follows, as shown in Figure **2**. First, a computer file of a model block is created, which contains a chain of inverters and buffers and a representative number of flip-flops **202**. (It will be understood that hereinafter references to creation of blocks or circuits, or their representation, and the like, refer to the creation and manipulation of computer files representing those entities and their associated parameters.) In this model block, V_{DD} and V_{SS} lines are provided, as well as a simple LR representation of the bondwire inductance and resistance. The specific circuit designed for this model will depend upon the block the model is designed to approximate. The idea is to allow an approximate representation of the signal switching, as it would occur over time during operation of the core block, by running a simulation of the model circuit. Second, the power and rms current, I_{rms}(model), of the core block are computed, for a clock frequency of f **204**. For this computation, the equation:

$$P=CV^2f=I_{rms}(model)V \quad \text{Eq. (1)}$$

is used, where P is the power of the block, C is the switching capacitance of the model block, and V is the voltage across it. Third, the I_{rms} and switching capacitance of the actual digital blocks in the chip, for example, a digital signal processor ("DSP") block, microprocessor block, glue logic block, custom macro block, etc., are computed **206** from the power value computed in step **204**. For this computation, the equation:

$$P=CV^2f=I_{rms}V \quad \text{Eq. (2)}$$

is used, where C is the capacitance of the actual digital block, and V is the voltage across it. Fourth, the number of instances N of the model block that are needed to match the actual computed power (or, equivalently, the I_{rms}) values (from step **206**) is computed **208**. For this computation, the equation:

$$N=I_{rms}/I_{rms}(model) \quad \text{Eq. (3)}$$

is used. Fifth, the model block is instantiated M times **210**. For this computation, the equation:

$$M=N/\alpha \quad \text{Eq. (4)}$$

is used, where α is a factor selected to reduce the simulation time. This step results in a decrease in the computed $I_{rms}(model)$ by the factor α. To compensate for this, since a goal is to ~~tee~~ compute the root-mean square and peak-to-peak voltages, V_{rms} and $V_{pk\text{-}pk}$, respectively, seen at the power and ground lines, the bond wire L and R values are increased by the factor α, in order to maintain Ldi/dt+IR invariant. Decoupling capacitance is added between the power supply and ground of the model block, instantiated M times. The value of the decoupling capacitance is selected to be a value that can actually be added to the IC. For example, this value may be between two times and ten times the switching capacitance computed in step **206**, above. Finally, a transient SPICE analysis is run to provide the output voltage as a function of time, and the values V_{rms} and $V_{pk\text{-}pk}$ are computed **212**. This completes the estimation of the core noise **214**.

Please replace the paragraph beginning at page 9, line 23, with the following rewritten paragraph:

The I/O terminal of the substrate netlist is connected to the substrate connection of the I/O buffer schematic netlist. The substrate connection of the critical analog circuit, say the ADC circuit, for example, is connected to the corresponding terminal of the substrate network. Figure **3** shows an exemplary network **300** of this kind. A block **302** representing the substrate netlist of the IC floorplan, for example as derived from a commercial program, as mentioned above, is shown in the figure, as well as a block **308** representing the critical analog circuit, in this case an ADC circuit, including a netlist **304** ~~**302**~~ of the ADC circuit. Circuitry **306** representing the I/O buffer is also shown. The entire network, comprising the substrate netlist **302**, the I/O buffer **306**, with its load capacitance **310**, and the critical analog circuit **308** may be compared across different test cases, for example with and without backside connection, with and without guard rings, the electrostatic discharge ("ESD") V_{SS} ring being shorted to or separated from the scribe seal, and other options, as desired by one implementing and employing the present invention. Since the worst case scenario in the example chosen to explain this embodiment is that eight I/O buffers can switch simultaneously, eight I/O buffers are used, each driving the typical load of 40 pF that the exemplary IC embodiment would see. The backgate contacts of the I/O buffers are connected to an I/O access port of the substrate netlist, and the back gate contacts of the ADC sampling network are connected to the receptor (i.e., critical analog circuit) access port of the substrate netlist.